AMENDMENTS TO THE CLAIMS:

1. (Currently Amended) A semiconductor integrated circuit, comprising:

a plurality of banks, each having a plurality of memory cells, and capable of writing and reading n bits of data (where n is a positive integer) to and from the plurality of memory cells;

a plurality of input/output means, each capable of receiving a plurality of bits of data from an external circuit and outputting a plurality of bits of data to the external circuit;

an n/2-bit data bus, extending along the plurality of banks;

n bits of first data line pairs, each first data line pair being associated with each bank to transmit data between the associated bank and the data bus;

n/2 bits of second data line pairs, each second data line pair being associated with each first data line pair and each input/output means to transmit data between the data bus and the associated input/output means; and,

a plurality of switching means for connecting one of the banks with a predetermined one of the input/output means via the associated first data line pair and associated second data line pair, and with other input/output means via the other associated first data line pairs, the n/2 bit data bus and other second data line ~~pairs~~ pair, based on a control signal.

2. (Original) The semiconductor integrated circuit according to claim 1, wherein an input buffer to input data and an output buffer to output data are provided within each of the banks, and the input buffer and the output buffer are connected to the first data line pairs.

3. (Original) The semiconductor integrated circuit according to claim 1, wherein each of the input/output means includes an input/output interface circuit having a plurality of input/output terminals.

4. (Currently Amended) A semiconductor integrated circuit, comprising:

a plurality of banks, each having a plurality of memory cells, and capable of writing and reading n bits of data (where n is a positive integer) to and from the plurality of memory

cells;

a plurality of input/output means, positioned opposing the plurality of banks respectively, each input/output means capable of receiving a plurality of bits of data from an external circuit and of outputting a plurality of bits of data to the external circuit;

an n/2-bit data bus, extending along the plurality of banks between the plurality of banks and the plurality of input/output means;

a plurality of first data line pairs of n bits each, each first data line pair being associated with each input/output means and each bank, and extending between the associated bank and the data bus to transmits data between the associated bank and the data bus;

a plurality of second data line pairs of n/2 bits each, each second data line pair being associated with each first data line pair and each input/output means, and extending between the data bus and the associated input/output means to transmit data between the data bus and the associated input/output means; and,

a plurality of switching means, provided at connection sites of the first data line pairs and the second data line pairs with the data bus, for connecting one of the banks with a predetermined one of the input/output means via the associated first data line pair and associated second data line pair, and with other input/output means via the other associated first data line pairs, the n/2 bit data bus and other second data line ~~pairs~~ pair, based on a control signal.

5. (Original) The semiconductor integrated circuit according to claim 4, wherein an input buffer to input data and an output buffer to output data are provided within each of the banks, and the input buffer and the output buffer are connected to the first data line pairs.

6. (Original) The semiconductor integrated circuit according to claim 5, wherein each of the input/output means includes an input/output interface circuit having a plurality of input/output terminals.

Claims 7-9 (Canceled)